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| EXAMINER | |
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2662 | 6 |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/625,375 | HUNG ET AL. | |
| | Examiner | Art Unit | |
| | David Odland | 2662 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. The following is a response to the amendments filed on 01/12/2004.

### *Specification*

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Objections*

3. Claim 1 is objected to because of the following informalities: the claim recites "...including at least one pointer to a next location the main queue corresponding to a..." in line 9. This statement is of improper English grammar. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claim15 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites "...wherein the process of storing a plurality of transaction pointers corresponds to the first memory location in a broadcast queue..." There is a lack of antecedent

basis for the limitation 'the first memory location' and furthermore is it unclear what 'transaction pointers' are being referred to.

Claim 16 is rejected because it depends on claim 15

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3 and 7-10, are rejected under 35 U.S.C. 102(b) as being anticipated by Harriman et al. (USPN 5,898,687), hereafter referred to as Harriman.

Referring to claim 1, Harriman discloses a network switch (a network switch (see figures 1 and 2 and column 2 lines 13-41)) comprising a first media access controller (MAC) (the switch comprises a CPU controller (see column 2 lines 13-41 and figures 1)) coupled to a plurality of ports (the CPU is coupled to a plurality of input and output ports (see column 2 lines 13-41 and items 102 and 104 in figures 1)), a transmitter coupled to the first MAC (an assembler is coupled to the CPU (see item 110 of figure 1)) and packet queuing control (PQC) coupled to the receiver (the receiver is coupled to a queuing control subsystem comprising, *inter alia*, an Input Translation Function (IFT), unicast queues, shared memory and a multicast engine (see items 120,130,112 and 200 in figure 1)), wherein the PQC includes a main queue for storing information corresponding to one or more data packets to be transmitted from the network switch as unicast transactions (the queuing control subsystem comprises a shared memory which is used

for storing the payload of unicast and multicast packets that are to be transmitted (see item 130 in figure 1)) and a broadcast queue, for storing information corresponding to one or to more data packets to be transmitted from the network switch as broadcast transactions (the multicast engine includes a plurality of multicast queues, which store the address pointers that point to locations in the shared memory that hold the payload of the next cell to be multicast (see column 5 lines 49-60 and items 200 and 240 in figures 1 and 2)), said information including at least one pointer to a next location in the main queue corresponding to a memory location from which data is to be transmitted (the multicast queues store the address pointers that point to locations in the shared memory that hold the payload of the next cell to be multicast (see column 5 lines 49-60 and items 200 and 240 in figures 1 and 2)). Note: since the CPU is controls the network switch, it also controls the access of incoming data to the output ports and ultimately to a transmission medium, therefore it can be considered a Media Access Controller (MAC).

Referring to claim 8, Harriman discloses a packet queuing control (PQC) a queuing control subsystem comprising, *inter alia*, an Input Translation Function (IFT), unicast queues, shared memory and a multicast engine (see items 120,130,112 and 200 in figure 1)) comprising a main queue for storing information corresponding to one or more data packets to be transmitted from a network switch as unicast transactions (a shared memory for storing the payload of unicast packets to be transmitted from a switch (see item 112 in figure 1)) and information corresponding to one or more data packets to be transmitted from the network switch as broadcast transactions (the shared memory also stores the payloads of packets that are to be transmitted as multicast packets (see item 112 in figure 1)) and a broadcast queue, for storing information corresponding to one or more data packets to be transmitted from a network switch

as broadcast transactions (the multicast engine includes a plurality of multicast queues, which store the address pointers that point to locations in the shared memory that hold the payload of the next cell to be multicast (see column 5 lines 49-60 and items 200 and 240 in figures 1 and 2)).

Referring to claims 2 and 9, Harriman discloses the system discussed above. Furthermore, Harriman discloses that the broadcast queue comprises a plurality of port queues, wherein each of the plurality of port queues corresponds to one of the plurality of ports (the multicast queues comprises a plurality of queues that each correspond to one of the output ports (see item 240 in figure 2)).

Referring to claims 3 and 10, Harriman discloses the system discussed above. Furthermore, Harriman discloses that the plurality of port queues comprise a first port queue for storing information corresponding to one or more data packets to be transmitted from a first of the plurality of ports (the multicast queue comprises a queue for each outgoing port (see the queue for port 0 in figure 2)) and a second port queue for storing information corresponding to one or more data packets to be transmitted from a second of the plurality of ports (the multicast queue comprises another queue for another one of the outgoing ports (see the queue for port 1 in figure 2)).

Referring to claim 7, Harriman discloses the system discussed above. Furthermore, Harriman discloses that the network switch further comprises address resolution logic (ARL) coupled to the PQC and the receiver (the ITF performs address translations, is coupled to the extractor and is part of the queuing control subsystem (see figure 1)) and a second MAC coupled to the receiver (an Output Translation Function (OTF) is also coupled to the receiver and

performs control operations (see column 2 lines 13-41 and figure 1)). Note since the OTF is partly in control of giving the incoming data to access to the output ports and ultimately a transmission medium, it can also be considered a Media Access Controller (MAC).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4-6 and 11-16, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman in view of Sato (USPN 6,009,078), hereafter referred to as Sato.

Referring to claims 4 and 11, Harriman discloses the system discussed above. Furthermore, Harriman discloses that the information stored in the broadcast queue includes a port number from which a data packet stored in a corresponding memory location is to be transmitted (the multicast queues have port numbers to which a corresponding packet, which is stored in a shared memory, will be transmitted from (see figures 1 and 2 and column 2 lines 13-41)).

Harriman does not disclose that the shared memory also stores the port numbers. However, Sato discloses a system wherein a common memory is used to store cells, their headers and next address pointers (see item 11 in figure 2). Implementing the shared memory, unicast queues and multicast queues all in a same memory of Harriman, in the manner taught by Sato, would be beneficial because doing so would require less development costs since only one memory is

being used rather than multiple memories. Furthermore, when accessing any memory there is an inherent delay called access-time, which is related to the time is takes to initiate communication with a memory, search the memory, retrieve data from the memory and transport the data to the appropriate processing element(s). Since Harriman stores the cell data in separate shared memory, unicast queues and multicast queues there will be a separate access-time required by each of the those memories, thus creating a significant delay compared to a single memory system, wherein only one access time delay may be afforded to the system. Therefore, for these reasons it would have been obvious to one skilled in the art at the time of the invention to combine the shared memory, unicast queues and multicast queues into a common memory, as taught by Sato, because doing so would reduce delay. This is especially important in Harriman because Harriman transmits ATM cells, which is used for the transport of data types such as audio and video data, which require low delay in order to maintain Quality-Of-Service conditions. Note, combing all the queues in this fashion means that the port numbers would also be in the same common memory.

Referring to claims 5,6,12 and 13, Harriman discloses the system discussed above. Furthermore, Harriman discloses that the information stored in the broadcast queue further includes a pointer to the next queue location from which a data packet stored in a corresponding memory location is to be transmitted (the multicast queues store pointers to the shared memory that stores the packet payloads that are next to be transmitted from the switch (see column 5 and 2 lines 13-41 and figures 1 and 2)); and

the pointers to a next queue are stored in the plurality of broadcast port queues for broadcast transactions (the multicast queues store pointers to the shared memory that correspond to packet payloads that are to be multicast (see column 2 lines 13-41 and figures 1 and 2)). Harriman does not disclose that the shared memory also stores the pointer to the next queue. However, Sato discloses a system wherein a common memory is used to store cells, their headers and next address pointers (see item 11 in figure 2). Implementing the shared memory, unicast queues and multicast queues all in a same memory of Harriman, in the manner taught by Sato, would require less development costs since only one memory is being used rather than multiple memories. Furthermore, when accessing any memory there is an inherent delay called access-time, which is related to the time is takes to initiate communication with a memory, search the memory, retrieve data from the memory and transport the data to the appropriate processing element(s). Since Harriman stores the cell data in separate shared memory, unicast queues and multicast queues there will be a separate access-time required by each of the those memories, thus creating a significant delay compared to a single memory system, wherein only one access time delay may be afforded to the system. Therefore, for these reasons it would have been obvious to one skilled in the art at the time of the invention to combine the shared memory, unicast queues and multicast queues into a common memory, as taught by Sato, because doing so would reduce delay. This is especially important in Harriman because Harriman transmits ATM cells, which is used for the transport of data types such as audio and video data, which require low delay in order to maintain Quality-Of-Service conditions. Note, combing all the queues in this fashion means that the next queue pointers would also be in the same common memory.

Referring to claim 14, Harriman discloses a method comprising receiving a first data packet at a first input port coupled to a network switch (packets arrive at the input ports of the network switch (see figure 1)), determining whether the first data packet is to be transmitted from the network switch as a unicast transaction (a determination is made as to whether the packet is to be unicast or multicast (see column 2 lines 13-41 and figure 1)) and if so, storing a pointer corresponding to the next location in the main queue corresponding to a memory location from which data is to be transmitted from the network switch (if the packet is to be unicast out of the switch, a pointer corresponding to the packet is stored in a unicast queue, wherein the pointer points to a location in a shared memory that stores the corresponding packet payload (see column 2 lines 13-41 and figure 1)), otherwise, storing a plurality of pointers in a broadcast queue corresponding to one or more next locations in the main queue corresponding to a memory location from which data is to be transmitted from the network switch (if the packet is to be multicast then a plurality of pointers corresponding to the packets are stored in the multicast queue (see figure 2)).

Harriman does not disclose that the shared memory also stores the pointer to the next location in the shared memory. However, Sato discloses a system wherein a common memory is used to store cells, their headers and next address pointers (see item 11 in figure 2). Implementing the shared memory, unicast queues and multicast queues all in a same memory of Harriman, in the manner taught by Sato, would require less development costs since only one memory is being used rather than multiple memories. Furthermore, when accessing any memory there is an inherent delay called access-time, which is related to the time is takes to initiate communication with a memory, search the memory, retrieve data from the memory and transport the data to the

appropriate processing element(s). Since Harriman stores the cell data in separate shared memory, unicast queues and multicast queues there will be a separate access-time required by each of the those memories, thus creating a significant delay compared to a single memory system, wherein only one access time delay may be afforded to the system. Therefore, for these reasons it would have been obvious to one skilled in the art at the time of the invention to combine the shared memory, unicast queues and multicast queues into a common memory, as taught by Sato, because doing so would reduce delay. This is especially important in Harriman because Harriman transmits ATM cells, which is used for the transport of data types such as audio and video data, which require low delay in order to maintain Quality-Of-Service conditions. Note, combing the shared memory and queues in this fashion means that the next location pointer will also be in this same common memory.

Referring to claim 15, Harriman discloses the system discussed above. Furthermore, Harriman discloses that the process of storing a plurality of transaction pointers corresponding to the first memory location in a broadcast queue comprises storing the pointer in a first port queue in the broadcast queue (the pointer is stored in a queue for port number 0 (see figure 2)), wherein the first port queue corresponds to a first output port coupled to the network switch (the port 0 queue corresponds to output port 0 of the switch (see figures 1 and 2)) and storing the pointer in a second port queue in the broadcast queue (the pointer is also stored in a queue for port number 1 (see figure 2)), wherein the second port queue corresponds to a second output port coupled to the network switch (the port 1 queue corresponds to output port 1 of the switch (see figures 1 and 2)).

Referring to claim 16, Harriman discloses the system discussed above. Furthermore, Harriman discloses transmitting the first data packet from the network switch via the first output port (the multicast packet is output from port 0 (see figures 1 and 2)) and transmitting the first data packet from the network switch via the second output port (the multicast packet is also output from the port 1 (see figures 1 and 2)).

***Response to Arguments***

10. Some of the Applicant's arguments filed 01/12/2004 have been fully considered but they are not persuasive.

On pages 11 and 12 regarding claim 1, the Applicant contends that Harriman does not teach storing a pointer too a next location in the main queue in the broadcast queue. The Examiner respectfully disagrees. Harriman discloses that the multicast queues store the address pointers that point to locations in the shared memory that hold the payload of the next cell to be multicast (see column 5 lines 49-60 and items 200 and 240 in figures 1 and 2).

On page 12, the Applicant also argues that Harriman does not teach a main queue that stores both unicast and broadcast information. The Examiner respectfully disagrees. Harriman discloses that a shared memory stores cell payloads of cells that are to be unicast or multicast (see column 5 lines 49-60 and items 200 and 240 in figures 1 and 2).

Applicant's arguments with respect to claims 14-16 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Odland, who can be reached at (703) 305-3231 on Monday – Friday during the hours of 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached at (703) 305-4744. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, who can be reached at (703) 305-4750.

deo

March 8, 2004

JOHN PEZZLO
PRIMARY EXAMINER